R18

Code No: 153AN

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, February -2024

DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	Given that $(16)_{10} = (100)_b$, and $(292)_{10} = (1204)_b$ determine the value of b.	[2]
b)	Draw AND gate using (i) NAND and (ii) NOR gate.	[3]
c)	What are don't care conditions?	[2]
d)	Draw full adder circuit in terms of half adder and write its truth table.	[3]
e)	What is triggering? List the types of triggering.	[2]
f)	Distinguish between a shift register and counter.	[3]
g)	Write about synthesis of synchronous sequential circuit.	[2]
h)	What is state diagram? Give an example.	[3]
i)	Define noise margin and figure of merit.	[2]
j)	Draw CMOS NAND gate.	[3]

PART – B

(50 Marks)

2.a) What is 2's compliment? Perform the subtraction operation using 2's complement representation $(84)_{10} - (63)_{10}$.

b) Prove that (i) $A + \overline{A}B = A + B$ (ii) (A + B) (A + C) = A + BC. [4+6]

OR

3.a) Convert the following Boolean expression $A\overline{B}C + \overline{A}\overline{B} + AB\overline{C}D$ into standard SOP form and $(\overline{A} + B + C)(\overline{B} + C + \overline{D})(A + \overline{B} + \overline{C} + D)$ into standard POS form.

b) Explain about parity check code and hamming code with an example for each. [6+4]

4.a) Simplify F(A,B,C,D) = $\sum$ (1,3,4,6,11) +d (0,8,10,12,13) using K-map and obtain minimum SOP.

b) What are hazards and hazard free relations? Explain. [7+3]

OR

5. Implement a full adder circuit with a) decoder and b) multiplexer. [10]

6. Compare the flip-flop excitation table for SR flip-flop and JK flip-flop. [10]

OR

7.a) Discuss about the operation of 4-bit left shift register.
b) Explain the operation of twisted ring counter. [5+5]

8.a) Discuss about mealy-type FSM for serial adder with state diagram.
b) Relate the operation of parity bit generator using moore model. [5+5]

OR

9. Design a synchronous sequential circuit that goes through the sequence 1,3,4,5,7 repeatedly. Use T flip flop for your design. [10]

10. Design a CMOS inverter and explain its operation. Comment on its characteristics such as Fan-in, Fan-out, Power dissipation, Propagation delay and Noise margin. Compare its advantages over other logic families. [10]

OR

11.a) Explain about TTL logic family.
b) Implement AND, OR and NOT gates using diodes and transistors. [4+6]

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